H-780-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Prior Application:	T. SAKATA et al Serial No. 09/349,761 Filed: July 9, 1999
Group Art Unit:	2133
Examiner:	J. Torres
For:	SEMICONDUCTOR INTEGRATED CIRCUIT WITH MEMORY REDUNDANCY CIRCUIT

PRELIMINARY AMENDMENT

Assistant Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Prior to examination, please amend the above-identified application as follows: